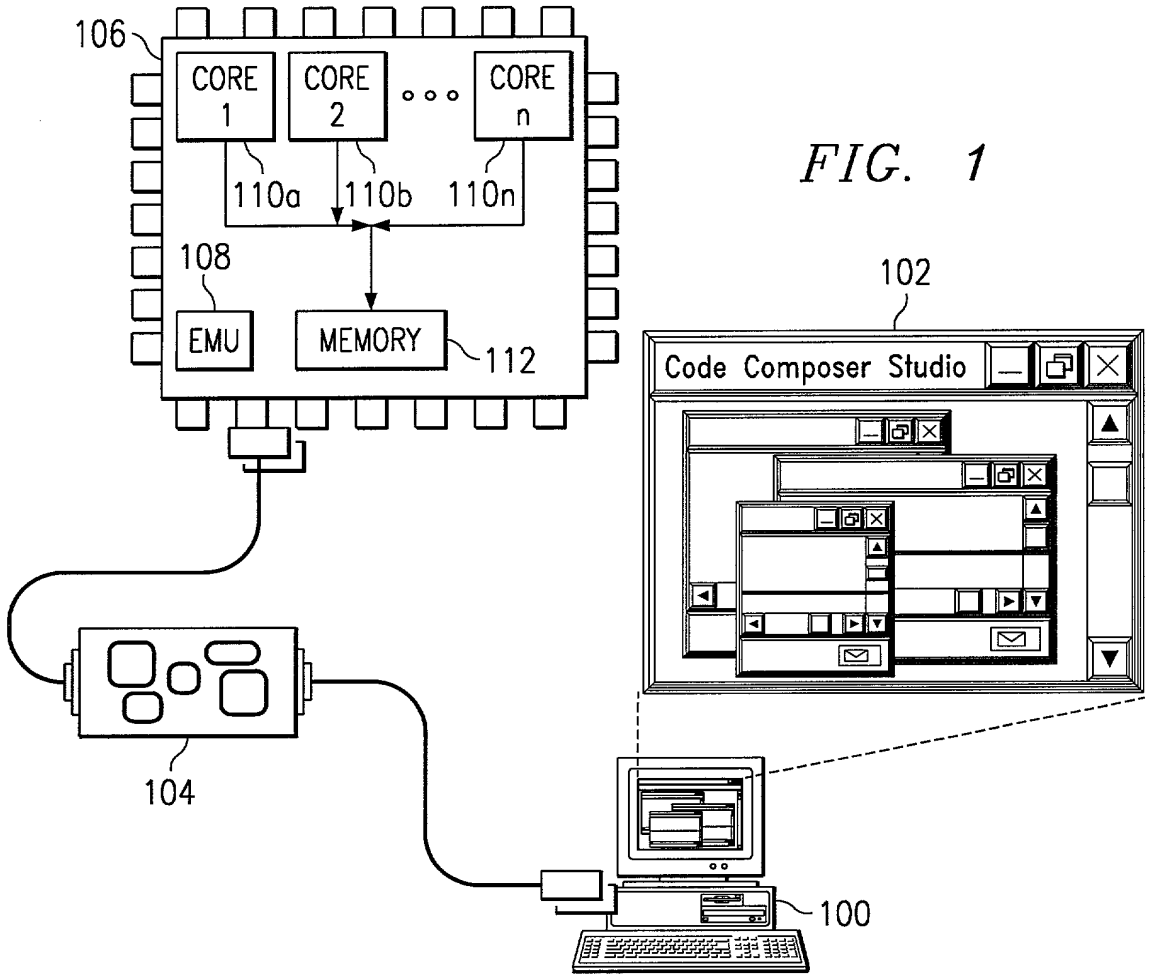

106
CORE 1
CORE 2
CORE n
110a
110b
110n
108
EMU
MEMORY
112
102
Code Composer Studio
104
100

FIG. 1

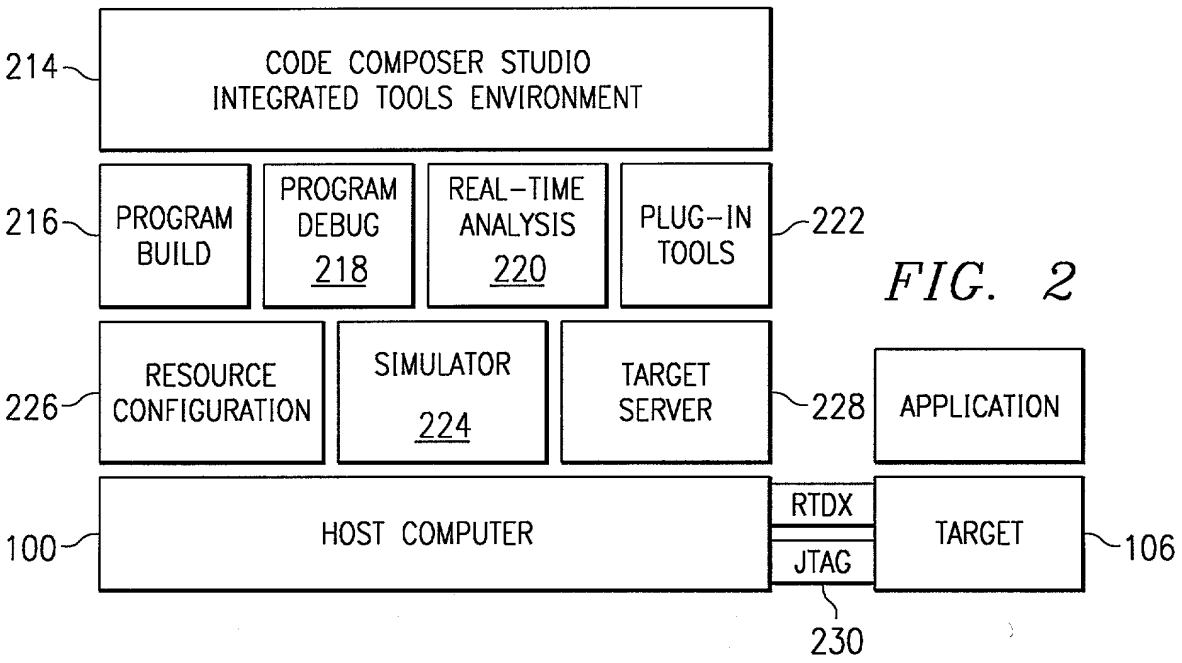
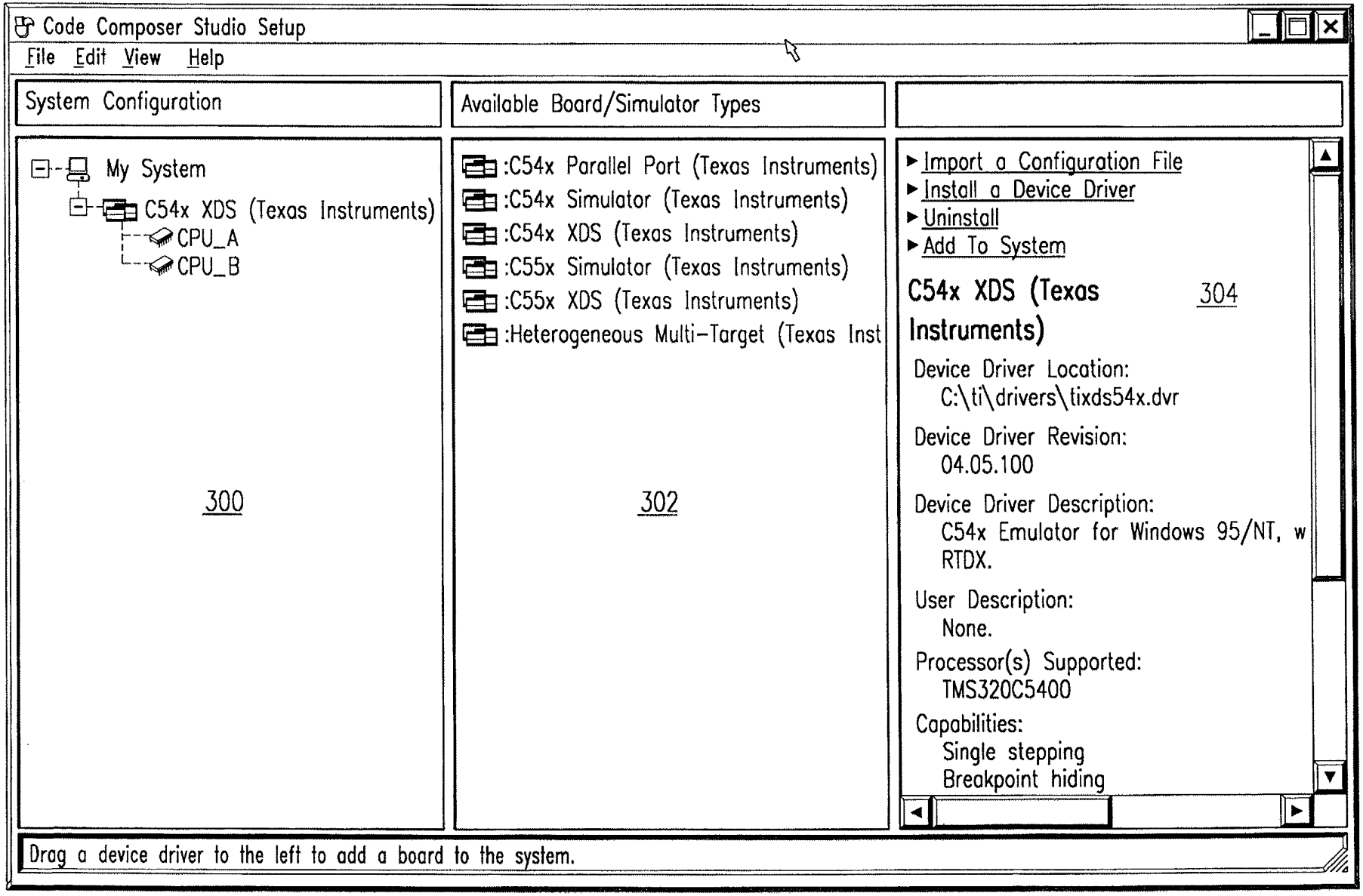

214
CODE COMPOSER STUDIO
INTEGRATED TOOLS ENVIRONMENT
216
PROGRAM BUILD
PROGRAM DEBUG 218
REAL-TIME ANALYSIS 220
PLUG-IN TOOLS
222
226
RESOURCE CONFIGURATION
SIMULATOR 224
TARGET SERVER
228
APPLICATION
100
HOST COMPUTER
RTDX
JTAG
230
TARGET
106

FIG. 2

FIG. 3


Code Composer Studio Setup
File Edit View Help
System Configuration
Available Board/Simulator Types
My System
C54x XDS (Texas Instruments)
CPU_A
CPU_B
300
:C54x Parallel Port (Texas Instruments)
:C54x Simulator (Texas Instruments)
:C54x XDS (Texas Instruments)
:C55x Simulator (Texas Instruments)
:C55x XDS (Texas Instruments)
:Heterogeneous Multi-Target (Texas Inst
302
Import a Configuration File
Install a Device Driver
Uninstall
Add To System
C54x XDS (Texas Instruments)
304
Device Driver Location:
C:\ti\drivers\tixds54x.dvr
Device Driver Revision:
04.05.100
Device Driver Description:
C54x Emulator for Windows 95/NT, w
RTDX.
User Description:
None.
Processor(s) Supported:
TMS320C5400
Capabilities:
Single stepping
Breakpoint hiding
Drag a device driver to the left to add a board to the system.

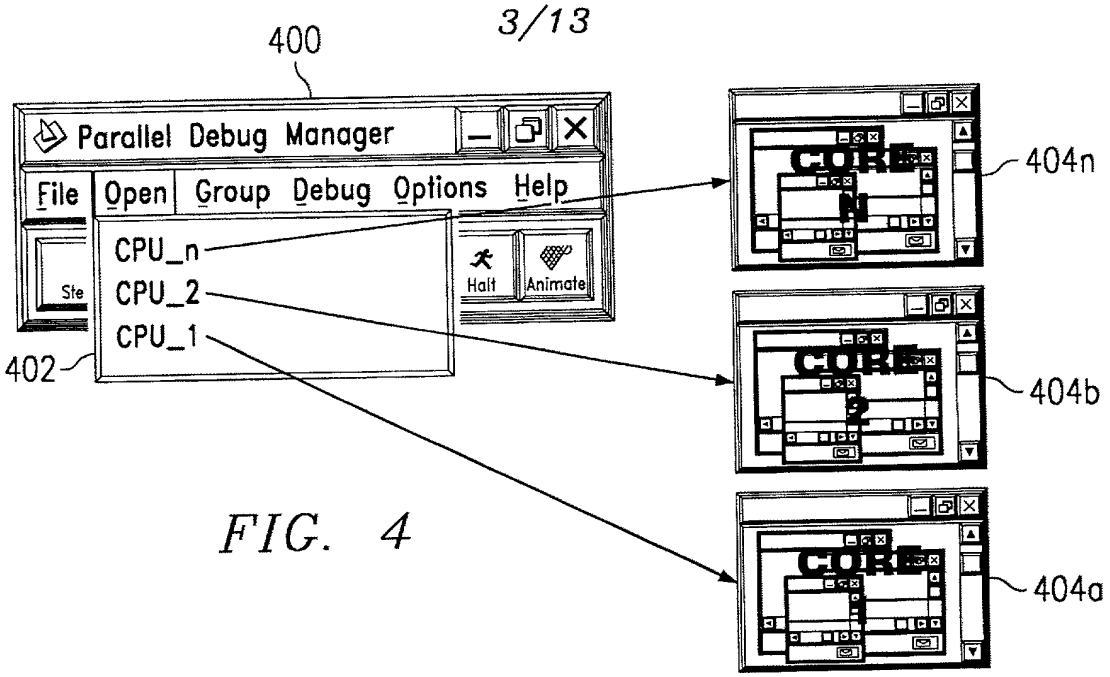

400
Parallel Debug Manager
File
Open
Group
Debug
Options
Help
CPU_n
CPU_2
CPU_1
Halt
Animate
402
404n
404b
404a

FIG. 4

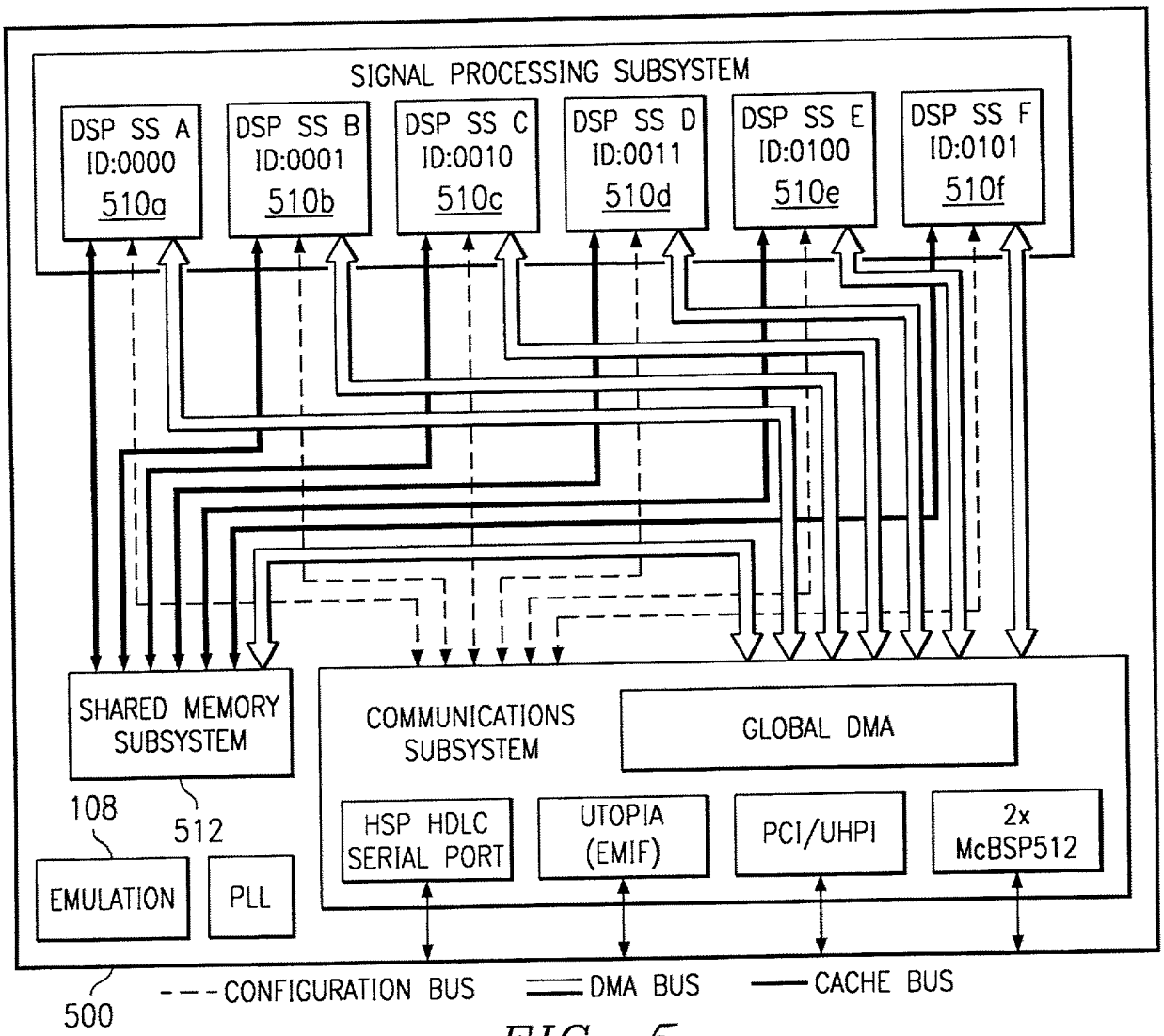

SIGNAL PROCESSING SUBSYSTEM
DSP SS A ID:0000 510a
DSP SS B ID:0001 510b
DSP SS C ID:0010 510c
DSP SS D ID:0011 510d
DSP SS E ID:0100 510e
DSP SS F ID:0101 510f
SHARED MEMORY SUBSYSTEM
108
512
EMULATION
PLL
COMMUNICATIONS SUBSYSTEM
GLOBAL DMA
HSP HDLC SERIAL PORT
UTOPIA (EMIF)
PCI/UHPI
2x McBSP512
500
CONFIGURATION BUS
DMA BUS
CACHE BUS

FIG. 5

FIG. 6

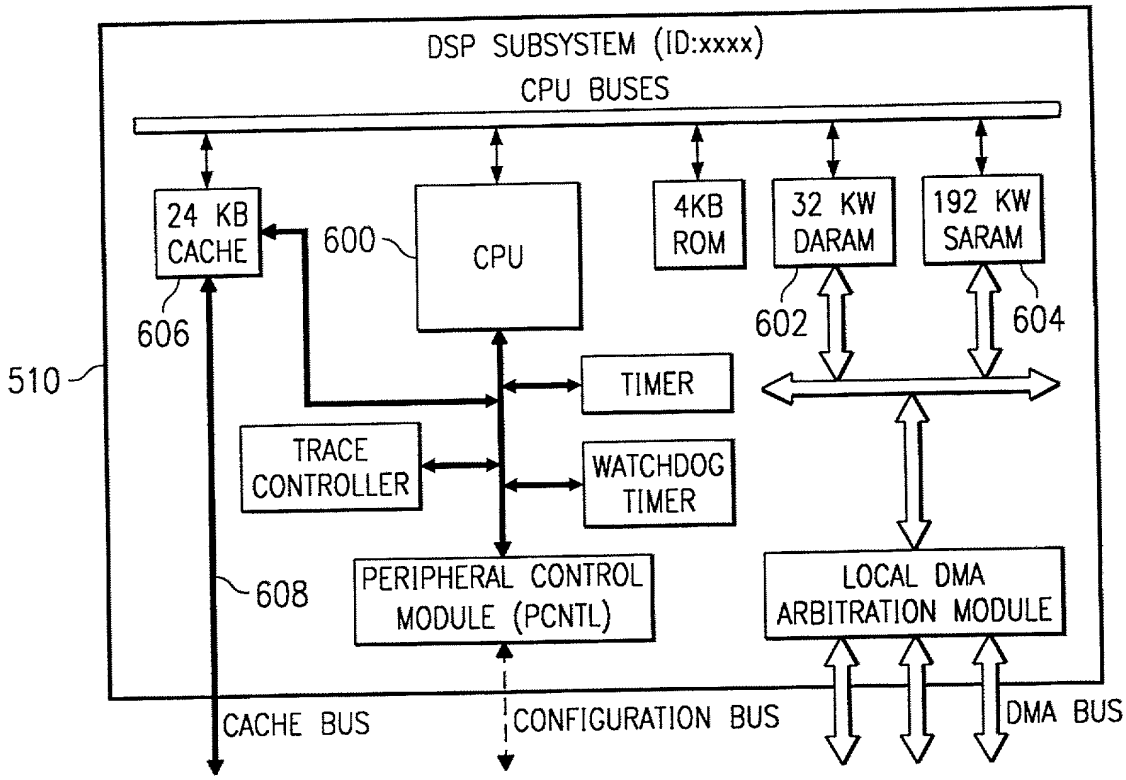
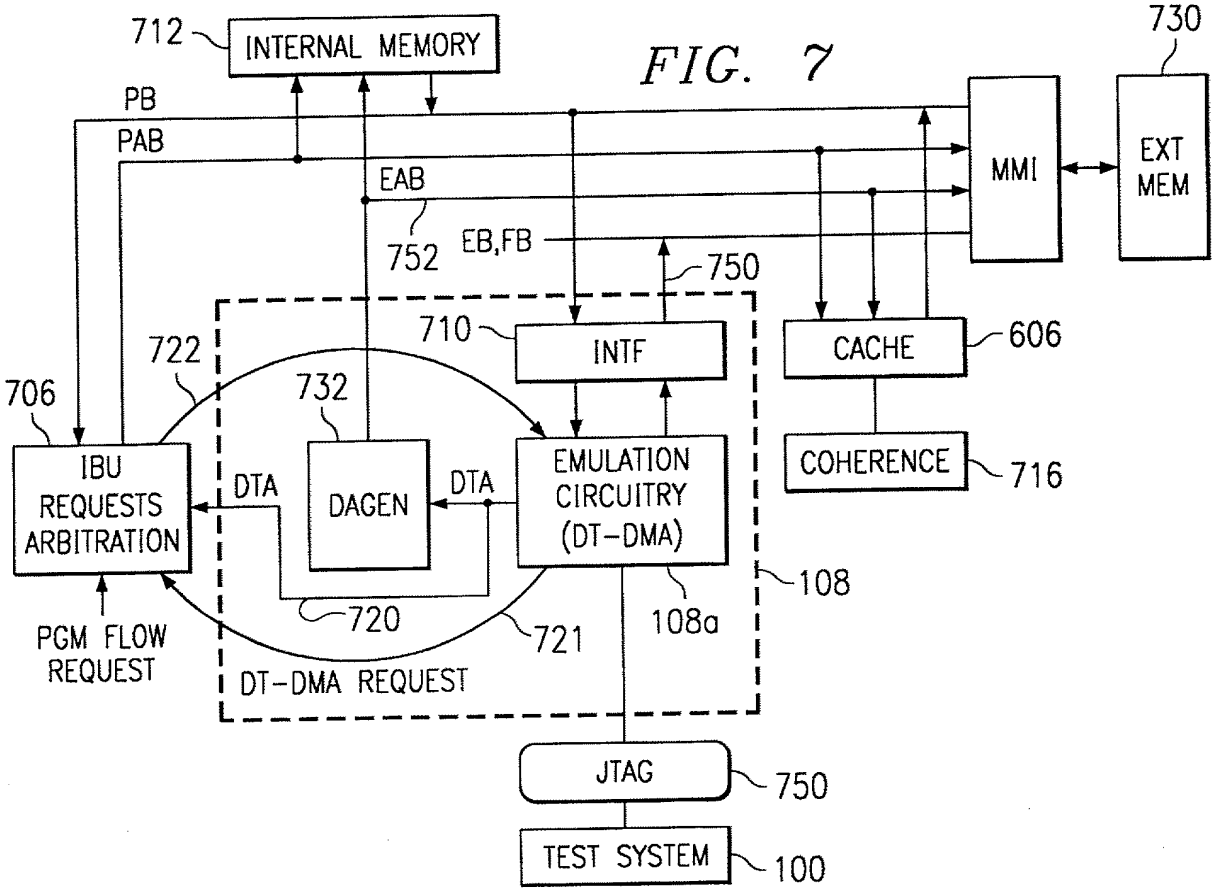

DSP SUBSYSTEM (ID:xxxx)
CPU BUSES
24 KB CACHE
606
600
CPU
4KB ROM
32 KW DARAM
602
192 KW SARAM
604
510
TIMER
TRACE CONTROLLER
WATCHDOG TIMER
608
PERIPHERAL CONTROL MODULE (PCNTL)
LOCAL DMA ARBITRATION MODULE
CACHE BUS
CONFIGURATION BUS
DMA BUS

FIG. 7


712
INTERNAL MEMORY
730
PB
PAB
EAB
752
EB,FB
MMI
EXT MEM
750
710
INTF
722
706
732
CACHE
606
IBU REQUESTS ARBITRATION
DTA
DAGEN
DTA
EMULATION CIRCUITRY (DT-DMA)
COHERENCE
716
108
720
721
108a
PGM FLOW REQUEST
DT-DMA REQUEST
JTAG
750
TEST SYSTEM
100

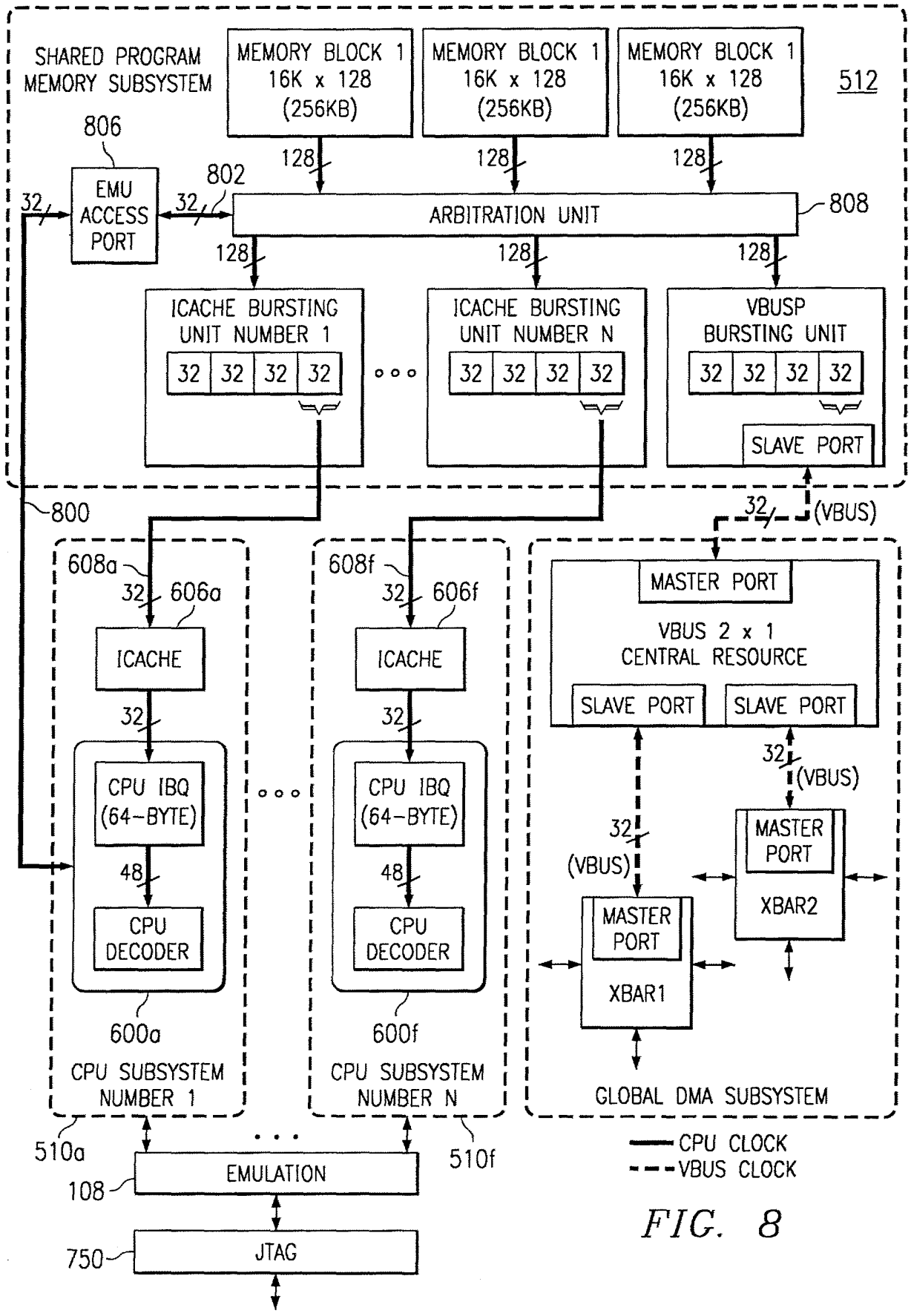
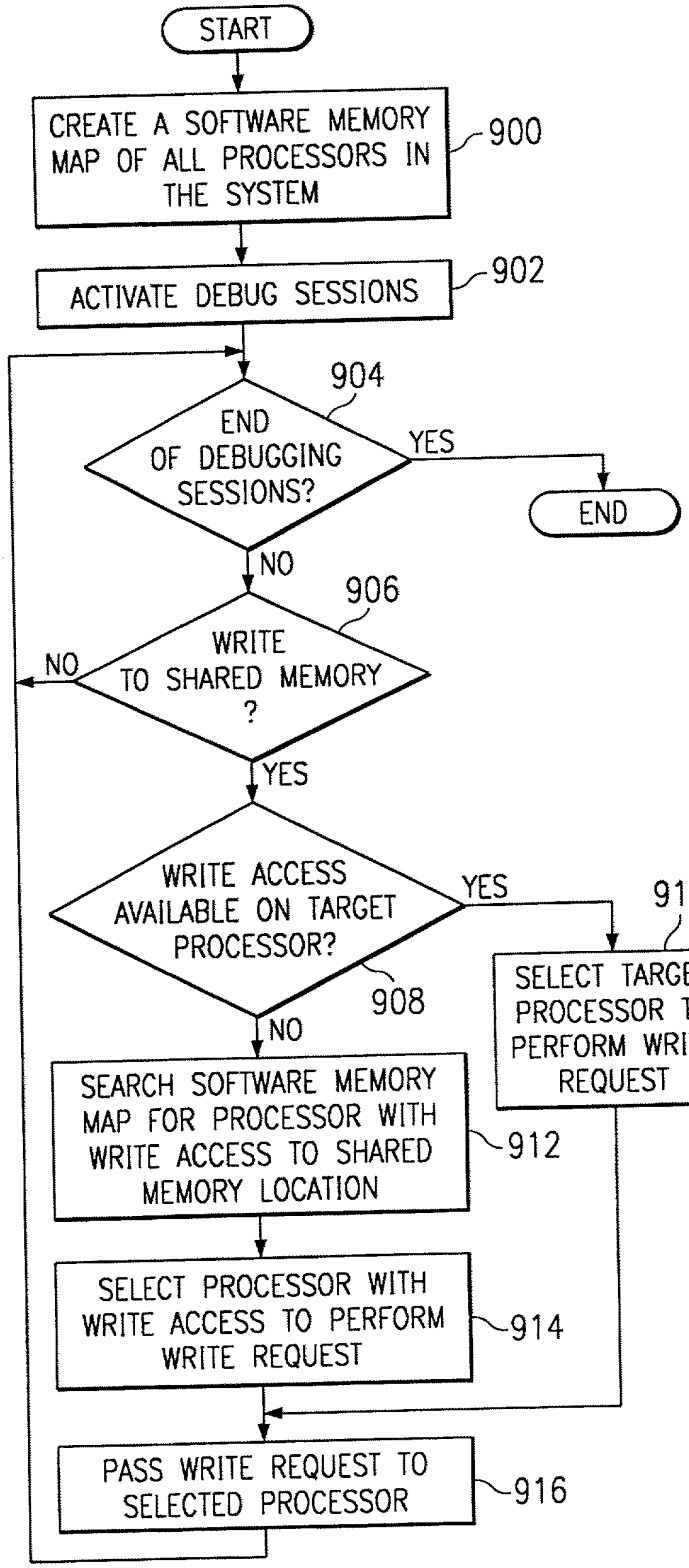

SHARED PROGRAM MEMORY SUBSYSTEM
MEMORY BLOCK 1 16K x 128 (256KB)
MEMORY BLOCK 1 16K x 128 (256KB)
MEMORY BLOCK 1 16K x 128 (256KB)
512
806
EMU ACCESS PORT
802
ARBITRATION UNIT
808
ICACHE BURSTING UNIT NUMBER 1
ICACHE BURSTING UNIT NUMBER N
VBUSP BURSTING UNIT
SLAVE PORT
800
608a
606a
ICACHE
CPU IBQ (64-BYTE)
CPU DECODER
600a
CPU SUBSYSTEM NUMBER 1
608f
606f
600f
CPU SUBSYSTEM NUMBER N
510a
510f
MASTER PORT
VBUS 2 x 1 CENTRAL RESOURCE
SLAVE PORT
XBAR1
XBAR2
GLOBAL DMA SUBSYSTEM
(VBUS)
CPU CLOCK
VBUS CLOCK
EMULATION
108
JTAG
750

FIG. 8

FIG. 9


START
CREATE A SOFTWARE MEMORY MAP OF ALL PROCESSORS IN THE SYSTEM
900
ACTIVATE DEBUG SESSIONS
902
904
END OF DEBUGGING SESSIONS?
YES
END
NO
906
WRITE TO SHARED MEMORY ?
NO
YES
WRITE ACCESS AVAILABLE ON TARGET PROCESSOR?
YES
910
908
NO
SELECT TARGET PROCESSOR TO PERFORM WRITE REQUEST
SEARCH SOFTWARE MEMORY MAP FOR PROCESSOR WITH WRITE ACCESS TO SHARED MEMORY LOCATION
912
SELECT PROCESSOR WITH WRITE ACCESS TO PERFORM WRITE REQUEST
914
PASS WRITE REQUEST TO SELECTED PROCESSOR
916

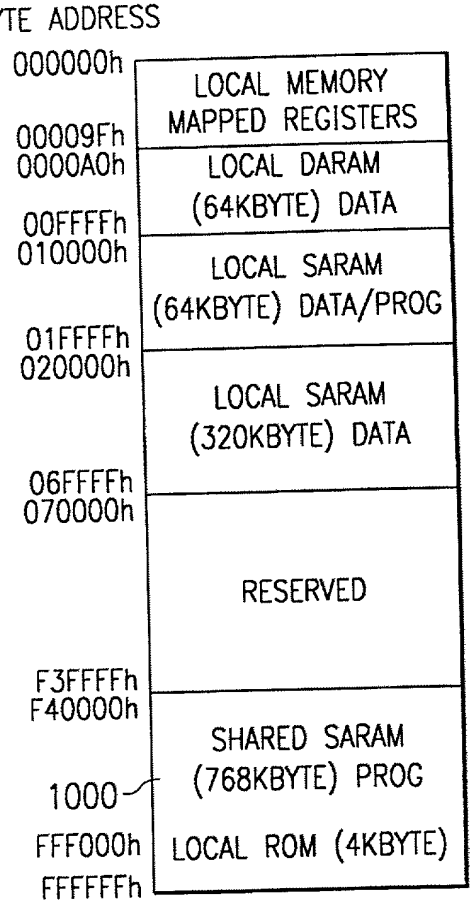

BYTE ADDRESS
000000h
LOCAL MEMORY MAPPED REGISTERS
00009Fh
0000A0h
LOCAL DARAM (64KBYTE) DATA
00FFFFh
010000h
LOCAL SARAM (64KBYTE) DATA/PROG
01FFFFh
020000h
LOCAL SARAM (320KBYTE) DATA
06FFFFh
070000h
RESERVED
F3FFFFh
F40000h
SHARED SARAM (768KBYTE) PROG
1000
FFF000h
LOCAL ROM (4KBYTE)
FFFFFFh

FIG. 10

FIG. 11

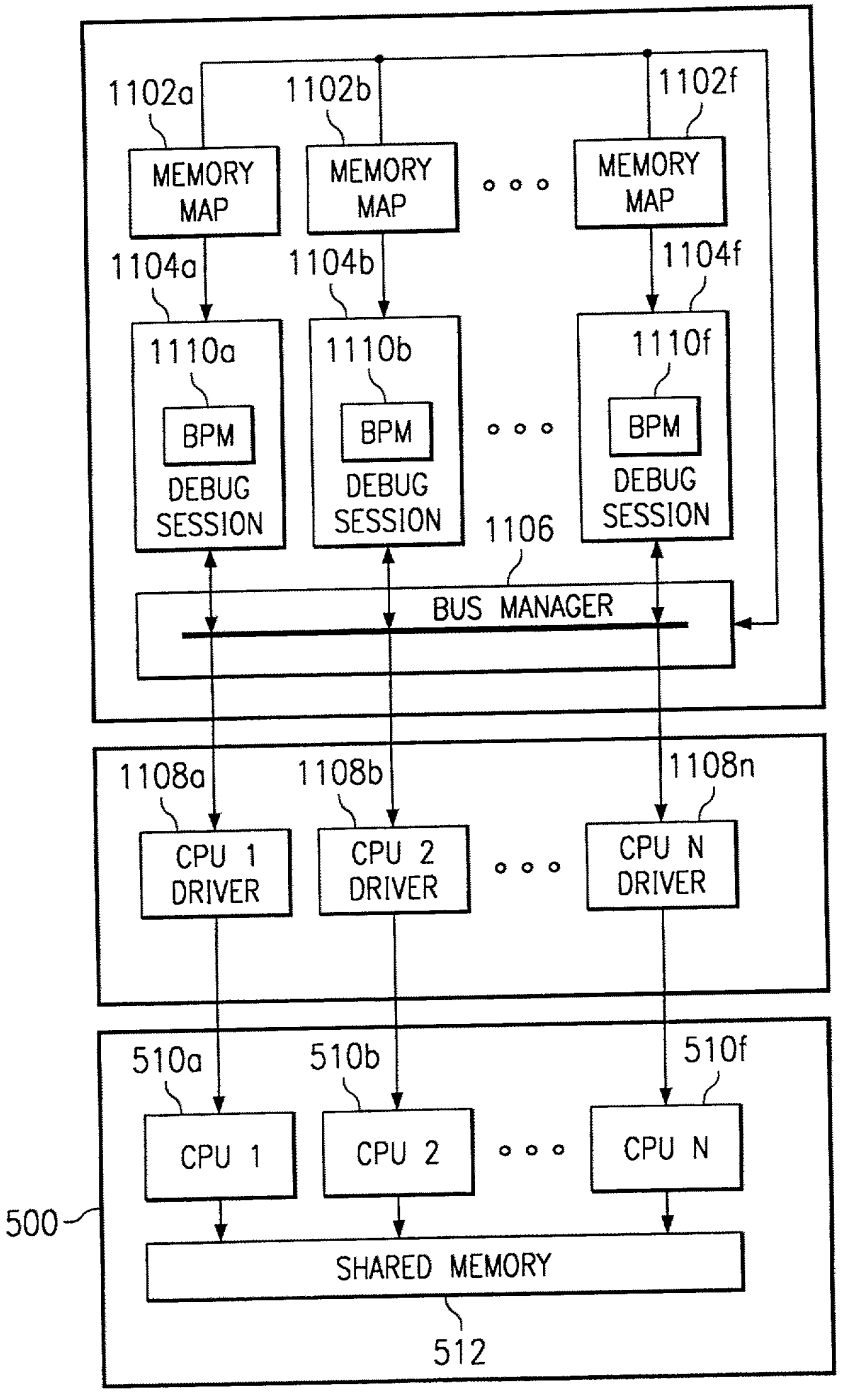

1102a
1102b
1102f
MEMORY MAP
MEMORY MAP
MEMORY MAP
1104a
1104b
1104f
1110a
1110b
1110f
BPM
DEBUG SESSION
BPM
DEBUG SESSION
BPM
DEBUG SESSION
1106
BUS MANAGER
1108a
1108b
1108n
CPU 1 DRIVER
CPU 2 DRIVER
CPU N DRIVER
510a
510b
510f
CPU 1
CPU 2
CPU N
500
SHARED MEMORY
512

FIG. 12A

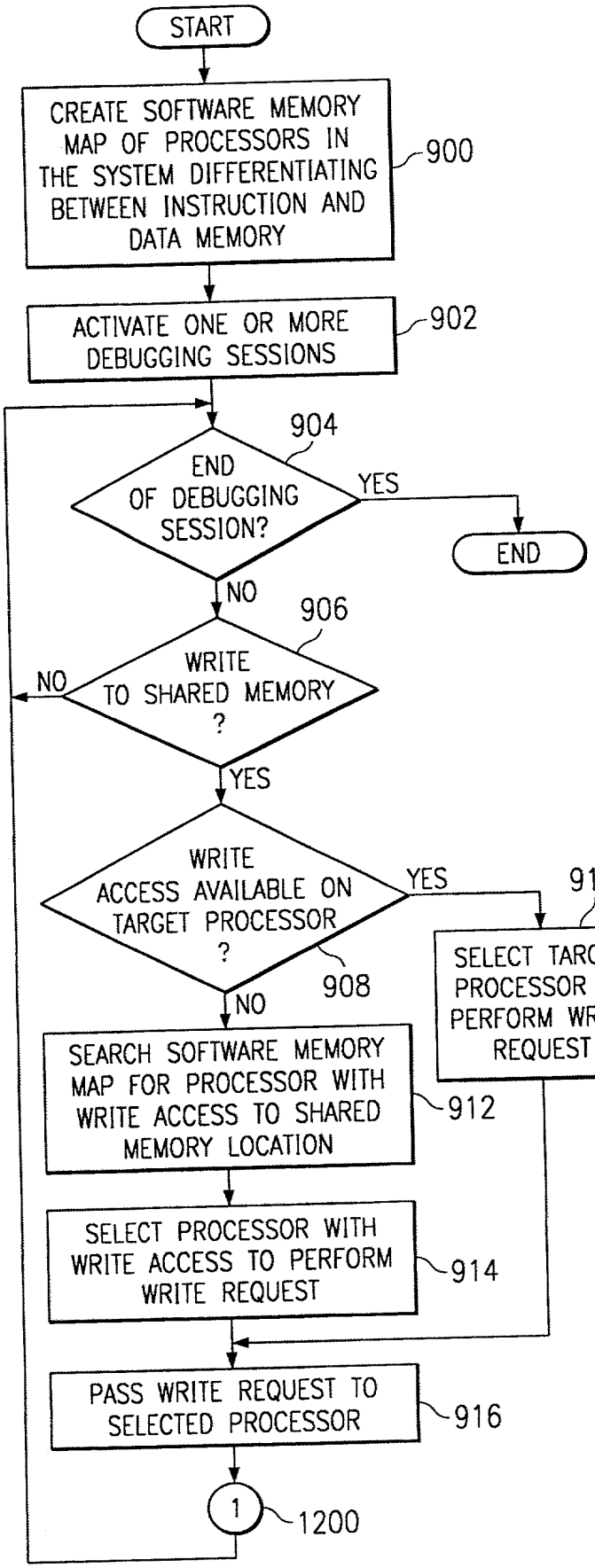


FIG. 12B

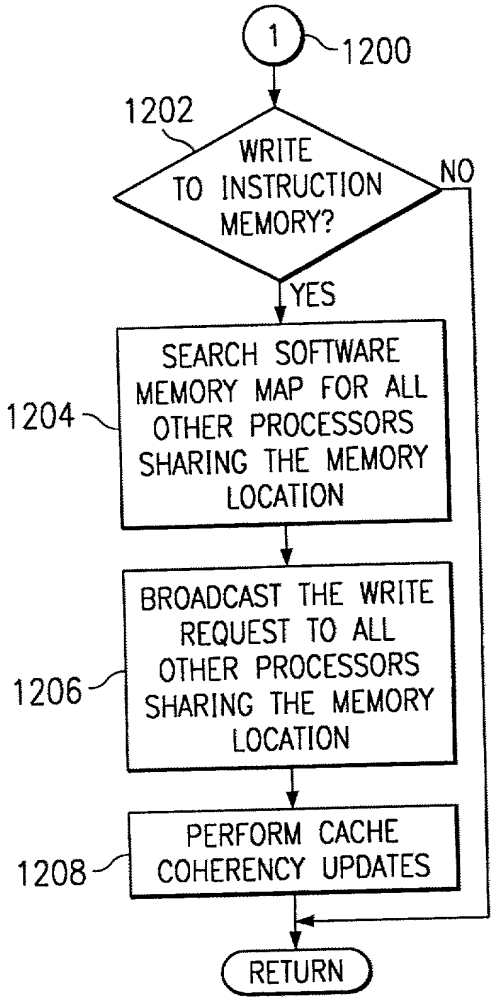


FIG. 13A

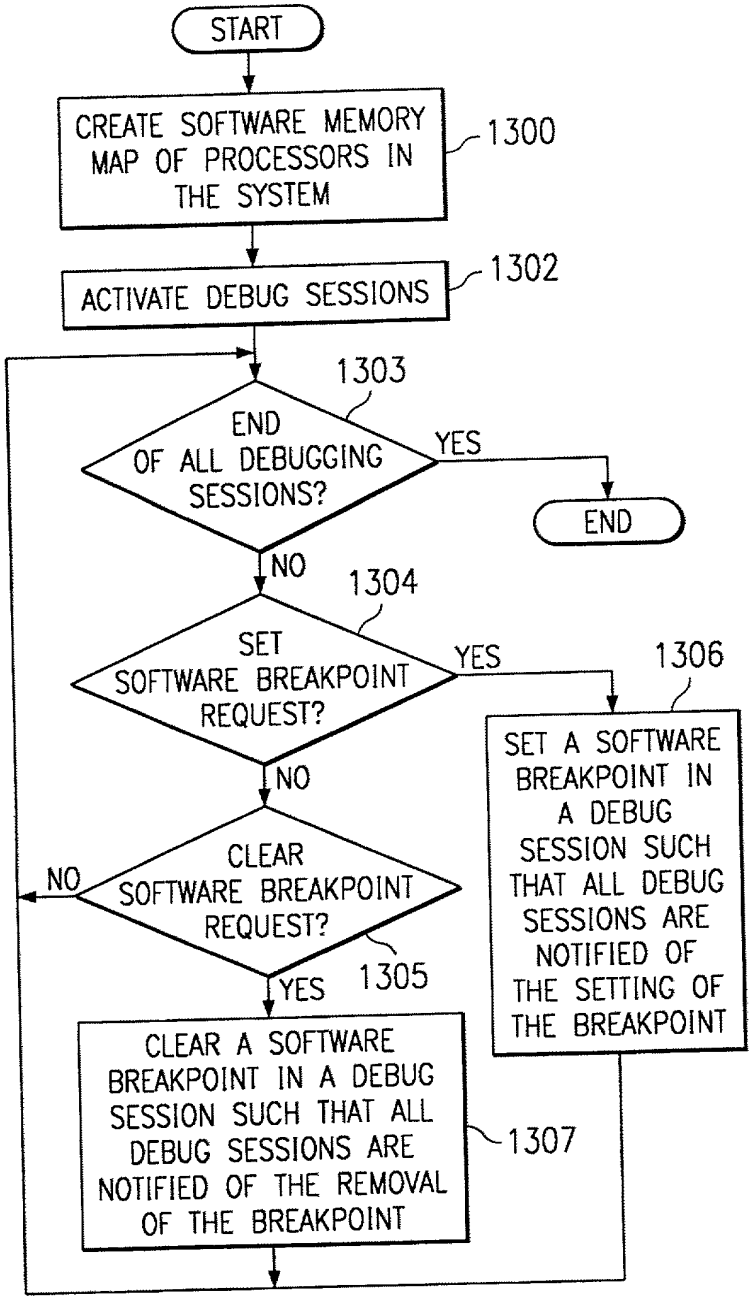


FIG. 13B

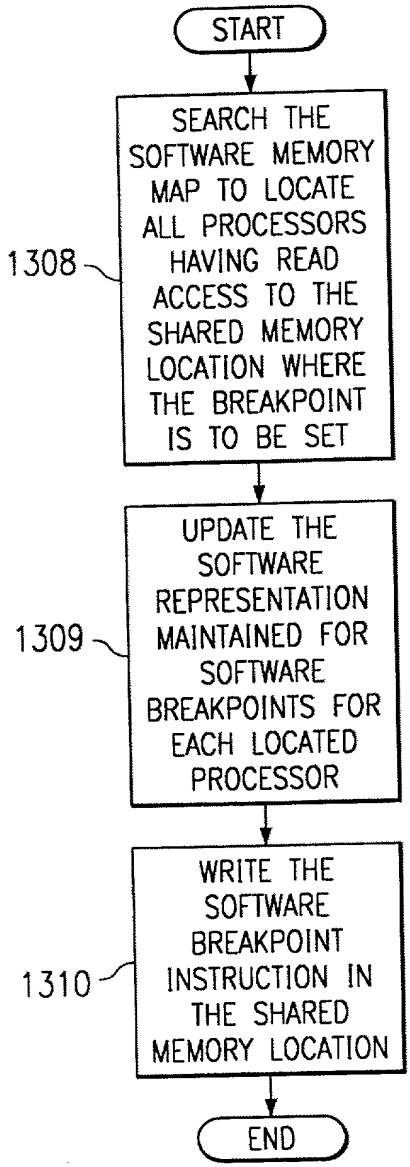


FIG. 13C

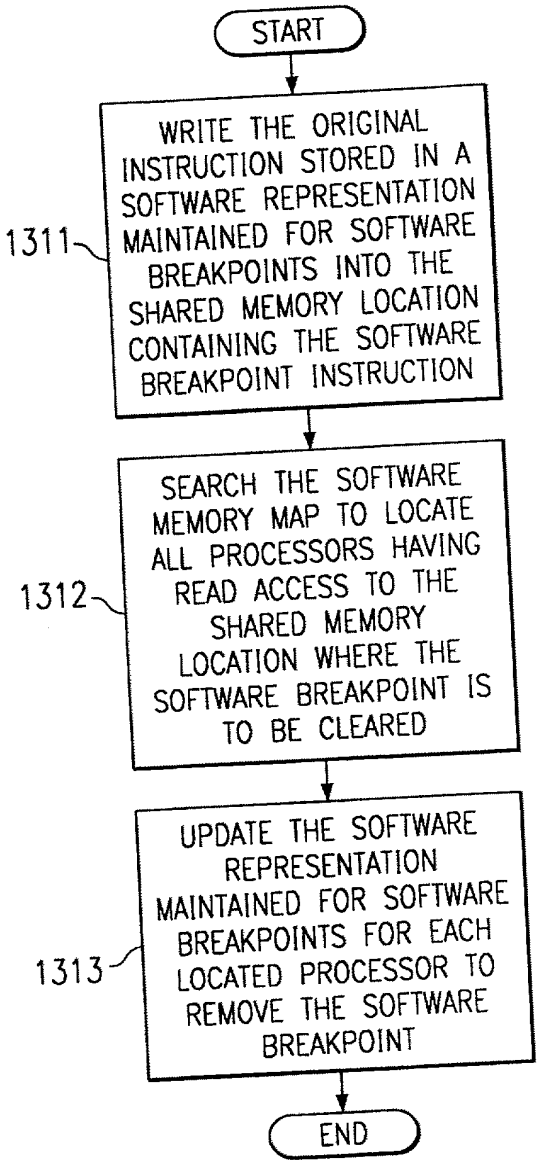
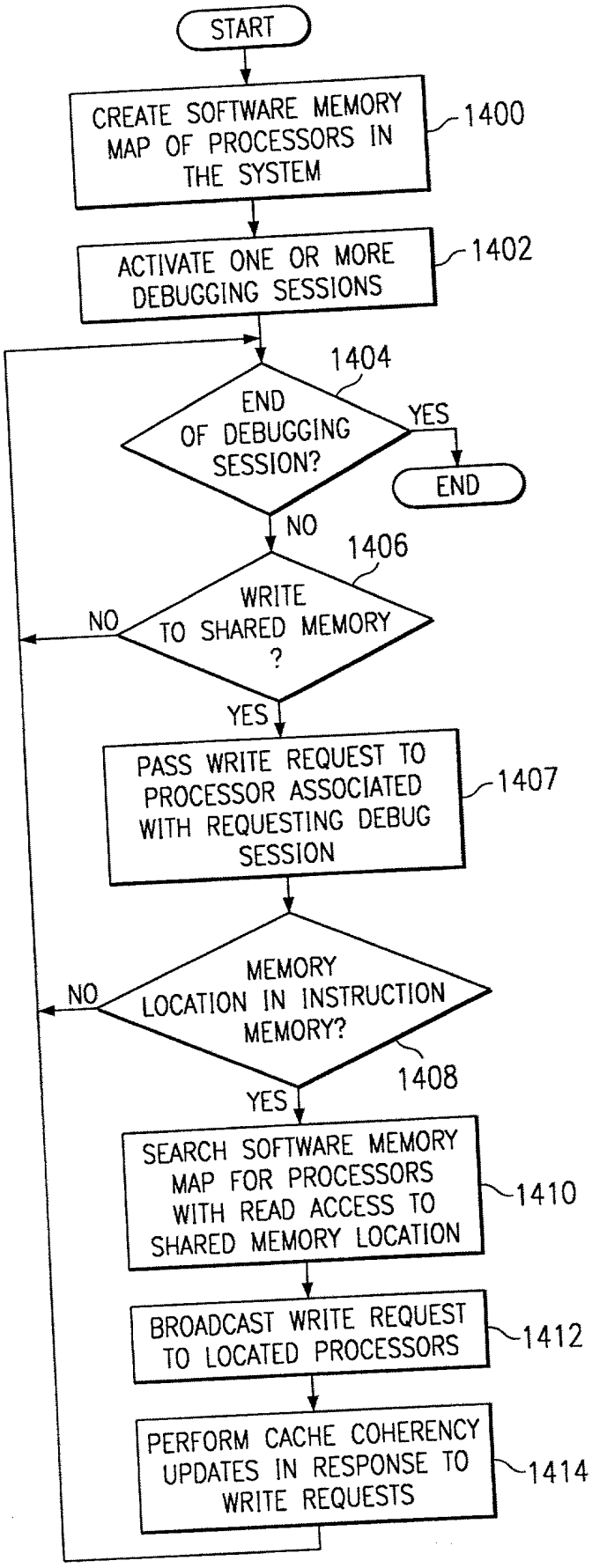


FIG. 14



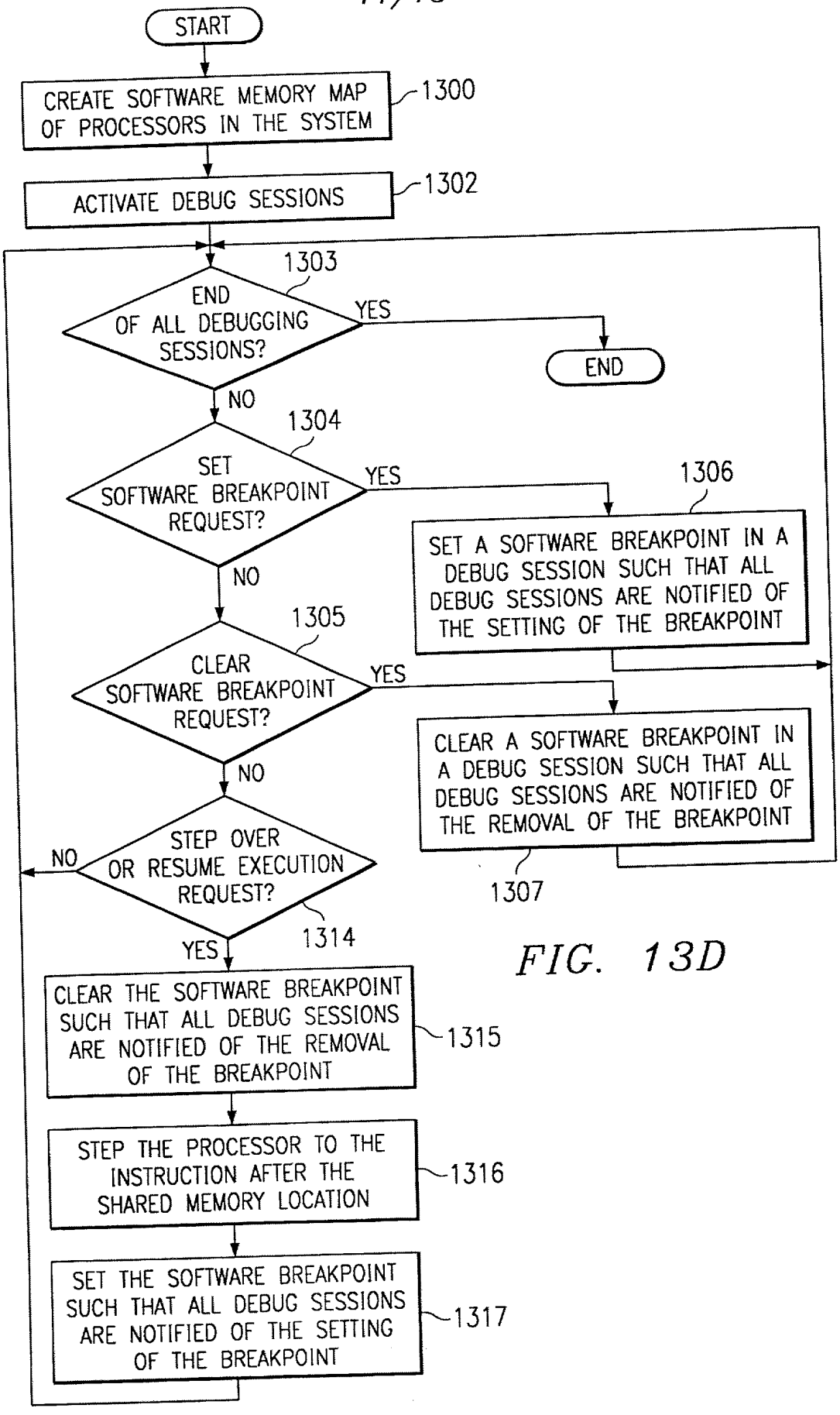

START
CREATE SOFTWARE MEMORY MAP OF PROCESSORS IN THE SYSTEM
1300
ACTIVATE DEBUG SESSIONS
1302
1303
END OF ALL DEBUGGING SESSIONS?
YES
END
NO
1304
SET SOFTWARE BREAKPOINT REQUEST?
YES
1306
SET A SOFTWARE BREAKPOINT IN A DEBUG SESSION SUCH THAT ALL DEBUG SESSIONS ARE NOTIFIED OF THE SETTING OF THE BREAKPOINT
NO
1305
CLEAR SOFTWARE BREAKPOINT REQUEST?
YES
CLEAR A SOFTWARE BREAKPOINT IN A DEBUG SESSION SUCH THAT ALL DEBUG SESSIONS ARE NOTIFIED OF THE REMOVAL OF THE BREAKPOINT
1307
NO
STEP OVER OR RESUME EXECUTION REQUEST?
NO
1314
YES
CLEAR THE SOFTWARE BREAKPOINT SUCH THAT ALL DEBUG SESSIONS ARE NOTIFIED OF THE REMOVAL OF THE BREAKPOINT
1315
STEP THE PROCESSOR TO THE INSTRUCTION AFTER THE SHARED MEMORY LOCATION
1316
SET THE SOFTWARE BREAKPOINT SUCH THAT ALL DEBUG SESSIONS ARE NOTIFIED OF THE SETTING OF THE BREAKPOINT
1317

FIG. 13D

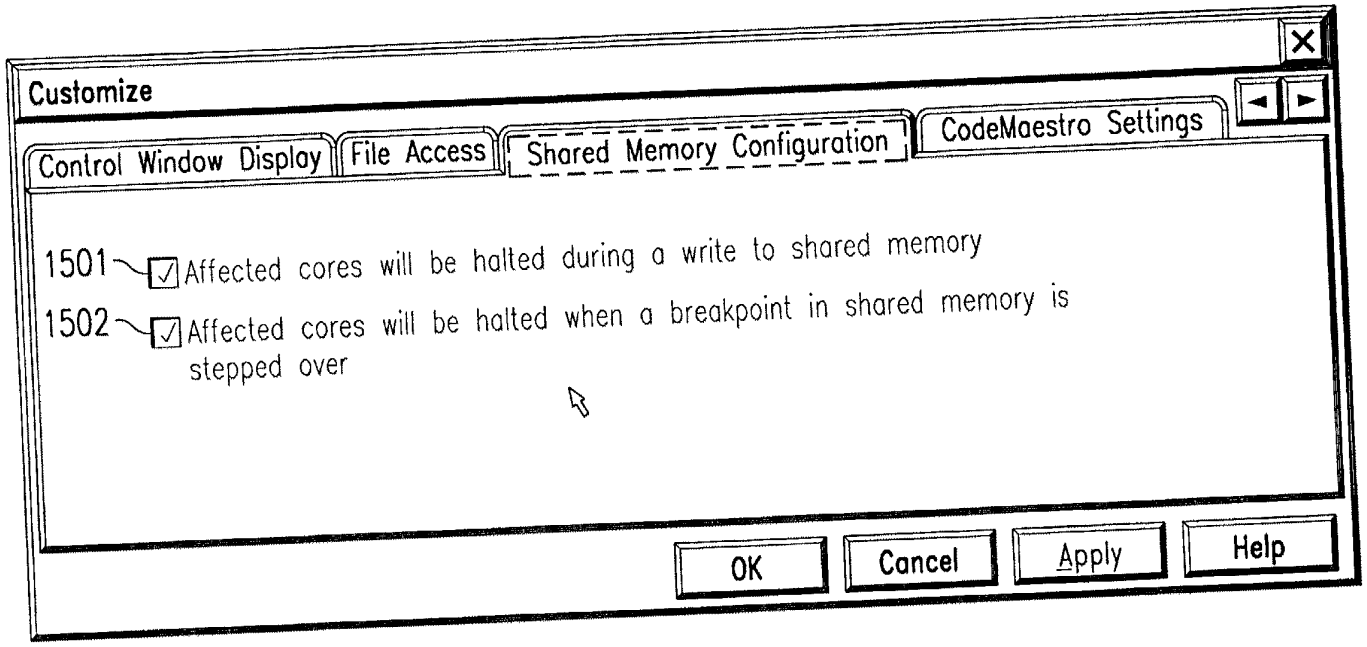


FIG. 15

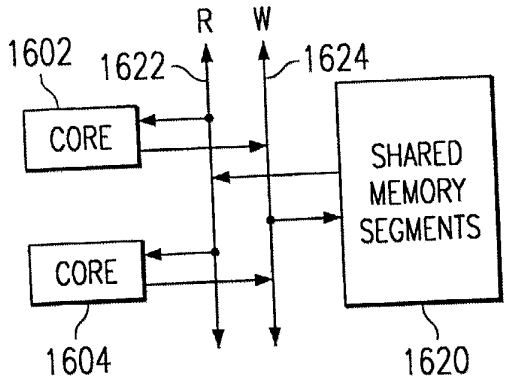


FIG. 16A

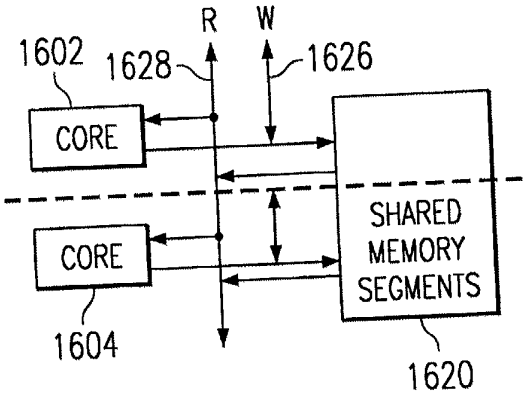


FIG. 16B

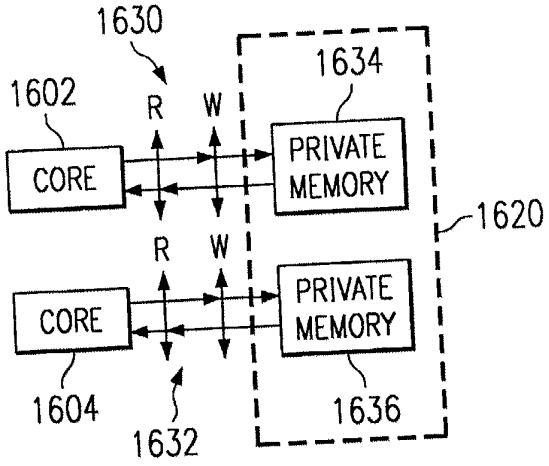
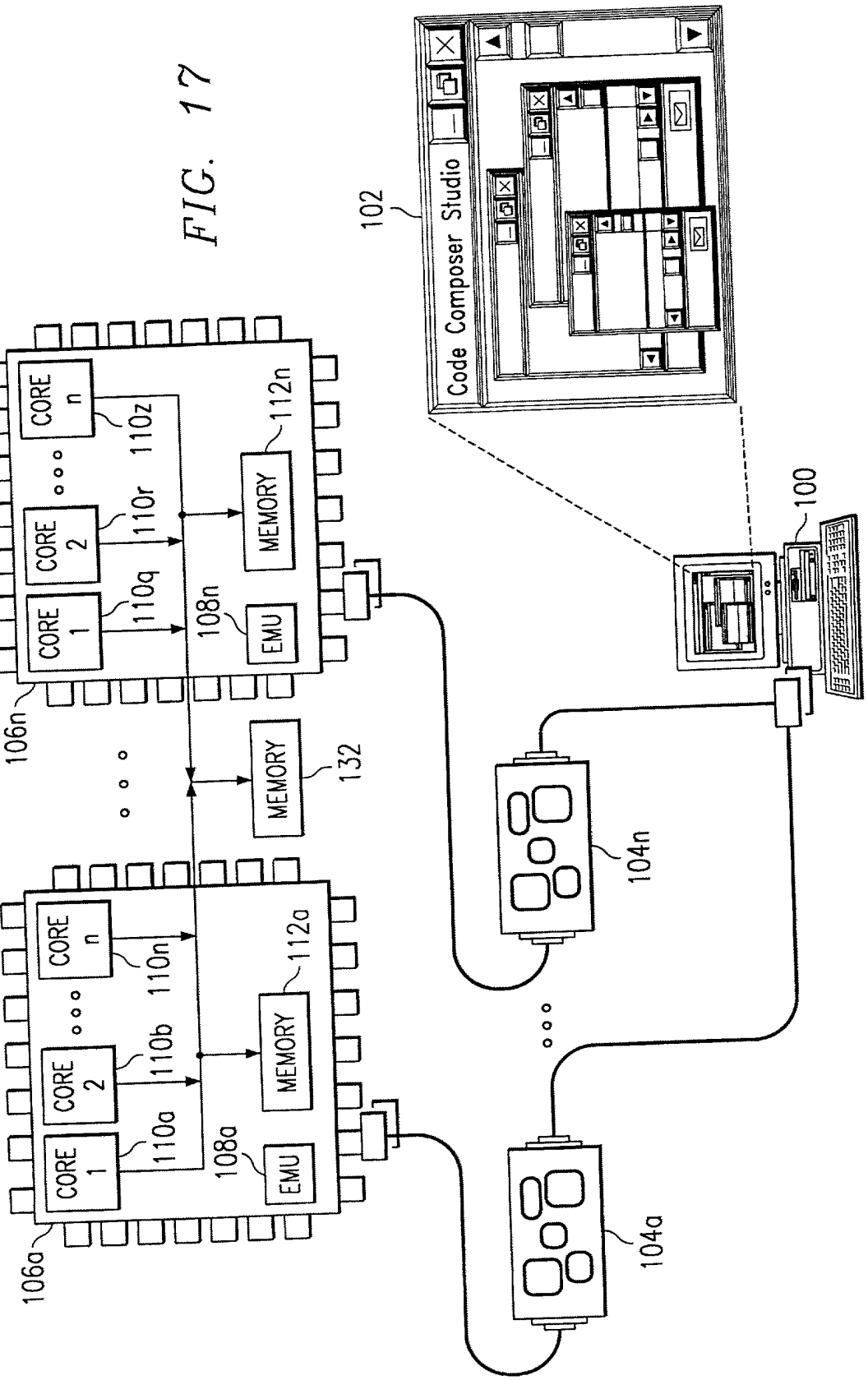


FIG. 16C

FIG. 17


Code Composer Studio
102
100
106n
106a
CORE 1
CORE 2
CORE n
110a
110b
110n
110q
110r
110z
108a
108n
EMU
MEMORY
112a
112n
132
104a
104n